

LISTING OF CLAIMS

*This listing of claims will replace all prior versions, and listings, of claims in the application:*

1. (Original) A content addressable memory, comprising:

multiple memory segments defining at least first and second memory segments;

and

a search control circuit configured to search the at least first and second memory segments in a prescribed order for certain data and to stop the search when the certain data is found.

2. (Original) The content addressable memory of claim 1, wherein the first memory segment is searched first, and the at least second memory segment is left unsearched if the certain data is found in the at least first memory segment.

3. (Original) The content addressable memory of claim 1, wherein each memory segment of the at least first and second memory segment comprises rows with a predetermined number of memory cells and columns with a predetermined number of memory cells which when combined together form a complete memory array.

4. (Original) The content addressable memory of claim 1, wherein at least one of the at least first and second memory segments comprises multiple memory segments.

5. (Original) The content addressable memory of claim 4, wherein the search control circuit is further configured to search all rows of each of the multiple memory segments searched.

6. (Original) The content addressable memory of claim 4, wherein the search control circuit is further configured to search all cells of all rows of each searched multiple memory segments.

7. (Original) The content addressable memory of claim 1, further comprising a circuit configured to allow all of the at least first and second memory segments to be searched regardless of whether the certain data is found in a particular memory segment.

8. (Original) The content addressable memory of claim 1, wherein the search control circuit comprises: a first search driver coupled to an input of the at least first memory segment; a first hit logic coupled to an output of the at least first memory segment; an extended search control coupled to an output of the first hit logic; a second search driver coupled to an output of the first search driver, an output of the extended search control, and an input of the at least second memory segment; and, a hit logic coupled to an output of the at least second memory segment.

9. (Original) The content addressable memory of claim 8, further comprising a hit arbiter coupled to the output of the first hit logic and the second hit logic and configured to produce a signal in accordance with whether the certain data is found.

10. (Original) The content addressable memory of claim 1, wherein the search control logic includes an extended search control circuit coupled to the first hit logic circuit and the second search control circuit and configured to receive a signal from the first hit logic circuit and cause the second search control circuit to begin a search of the at least second memory segment in accordance with the signal from the first hit logic circuit.

11. (Original) The content addressable memory of claim 8, further comprising a priority encoder coupled to the output of the first hit logic and the output of the second hit logic.

12. (Original) The content addressable memory of claim 1, further comprising a first search control circuit and a first hit logic circuit coupled to the at least first memory segment and a second search control circuit and a second hit logic circuit coupled to the at least second memory segment.

13. (Original) The content addressable memory of claim 1, further comprising the multiple memory cells organized into an array defining rows and columns of the content addressable memory, wherein the content addressable array is subdivided into memory segments along the dimension of the rows, and is not subdivided into memory segments along the dimension of the columns.

14. (Original) The content addressable memory of claim 1, further comprising an extended search control circuit coupled to the search driver.

Claims 15. – 17. (Canceled).

18. (Currently amended) A The content addressable memory of claim 15 comprising:

a first array of memory cells;

a second array of memory cells;

a search logic circuit configured to prevent the discharge of the second array of memory cells when a search of the first array of memory cells finds certain data,

wherein the search logic circuit comprises an extended search control circuit connected between the first array of memory cells and the second search driver, and

wherein the extended search control circuit is configured to control whether the second array of memory cells is searched based on whether certain data is found in the first array of memory cells.

Claim 19. – 20. (Canceled).

21. (Currently amended) A The method of searching a content addressable memory claim 19, further comprising the steps of:  
providing multiple memory cells in at least a first and second memory segment;  
searching the at least first memory segment for certain data; and  
stopping the search before searching the second memory segment if the certain data is found in the first memory segment; and

continuing the search in the second memory segment if the certain data is not found in the first memory segment.

Claims 22. – 24. (Canceled).

25. (Original) A method of searching a content addressable memory, comprising the steps of:

dividing the content addressable memory into at least a first and second memory segment;

searching the at least first memory segment before searching the at least second memory segment in a prescribed order for certain data;

wherein if the certain data is found in the first memory segment, stopping the search; and,

if the certain data is not found in the at least first memory segment continuing the search in the at least second memory segment.